# ROTORY DIODE FAILURE DETECTOR

*Vladimir Lalev, Kiril Banev, Bisser Borissov*

*Summary:* In relation to the modernization related to the power uprate of the units at Kozloduy NPP , the generator exciter has been replaced and the four signals have different amplitude and phase compared to the original signals. The failure detector is designed and set up to operate the original signals, which leads to problems in its operation as follows: spurious actuation of a signal for blown fuse (s) or, which is worse, failure to actuate the signal when the fuse is blown.

In order to prevent similar problems, a decision was taken to install a device for phase and amplitude correction to enable the change in the phase and amplitude of the signals.

*Key words:* rotory diodes, phase shift (correction), LabVIEW, FPGA

## 1. Introduction

The rotating rectifier is designed to rectify the current generated by the exciter, which is used for excitation of the main generator.

The rotating rectifier is based on the bridge diagram and is installed on the exciter shaft. It consists of 6 branches, each having 12 arms. Two rotor diodes, type D-105, with a set of units of resistances and condensers are connected in parallel to each of the bridge arms. One fuse, type PP-71M, is connected in parallel to every couple of the connected diodes (144 in total), Figure 1.

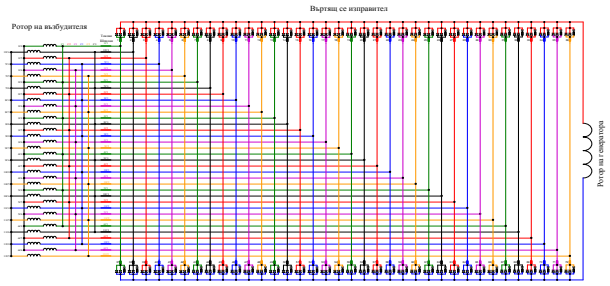


*Fig.1 Rotating rectifier - schematic diagram*

## 2. Excitation Control System

Fig. 2. shows the unit diagram of the excitation control system.

The instrumentation operates four sensors:

• Current sensors - two in operation and two in stand-by mode;

• Clock sensor - one in operation and one in stand-by mode;

• Cycle sensor - one in operation and one in stand-by mode;

The current sensors are flat induction elements in the shape of a rectangular frame. Four sensors are installed on the rotating rectifier, two at every

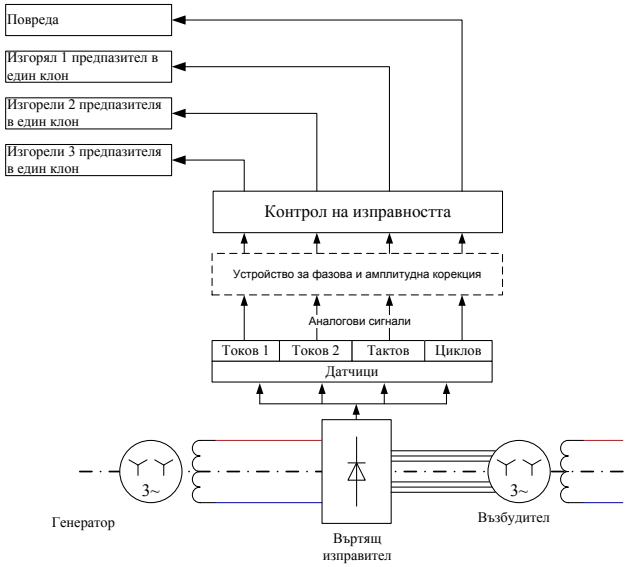


*Fig.2 Exciter control after the change - flowchart*

30°. When a electric current circuit is passing along the sensor, current depending on the current magnitude in the circuit is induced in its winding.

The clock (time) signal is in a phase with the measured current signals from the two current sensors. The current signal is used to start-up the A/D converter and obtain the real value of the current measured signals from the two current sensors.

The cycle sensor sends a signal for every shaft revolution. For every current sensor, there are 36 measuring points between the two cycle signals (one loop). Thus, every measured signal is designed to control 36 diodes of the rotating rectifier.

The clock and cycle sensors are operated according to the induction principle and are an inductive element of the U-shaped core with magnetic biasing from a permanent magnet. When there is a tooth opposite the sensor, a high level signal is generated at the exit, Figure 3.

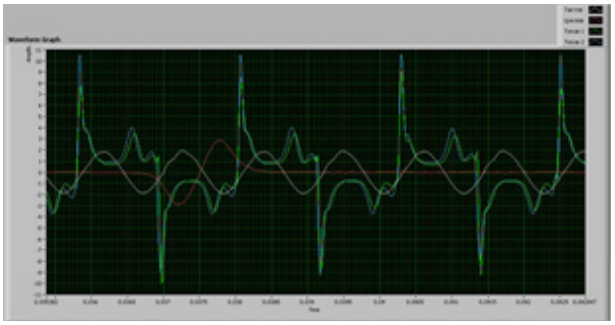

*Figure 3 Signals from exciter control system*

The real values of the measured signals from current sensors are compared to the averaged values for one period. If one of the signals from the current sensors is lower that the averaged value, the reference control device recognized that the relevant fuse of the rotating rectified has been blown.

The device defines the number of the blown fuses (1-6) in every arm of the rotating rectifier between the two cycle signals.

The device has four outputs, indicated the count of blown fuses in each branch.

## 3. Design of the device for phase and amplitude correction

The frequency of generator rotation is 25Hz , and one rotation is divided into 36 clock signals, i.e. 900 strokes per revolution It is selected to make 100 reports for a period, which means scanning frequency f=25·36·100=90000Hz.

Based on the performed analysis of the signals of the control system for the exciter, the conclusion is made that an independent system with RTOS and FPGA will be used. Figure 4 shows the FPGA structural diagram - these are device diagrams

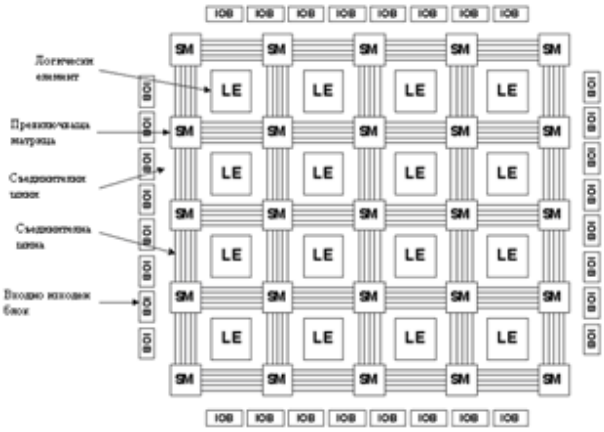


*Figure 4 FPGA structural diagram*

which can be modified in the process of their use. They consist of configurable logic blocks similar to the switches with many inputs, but one output. For digital diagrams these switches perform basic binary operations AND, NAND, OR, NOR and XOR.

As a result of the established requirements to the device for phase and amplitude correction and the performed review of the independent systems, a conclusion is made that for the installation of the device, an independent system with RT controller and FPGA is required.

The CompactRIO and Single-Board RIO meet these requirements, and because of the modular structure, i.e. possibility to select different input/ output device, the CompactRIO is selected– Figure 5.

*Figure 5 Rack NI cRIO-9063 with NI9215 and NI9263 modules*

Figure 6. shows the typical architecture of the software of the NI CompactRIO including:

• FPGA VI – a virtual instrument (VI), operated at FPGA including n-number of cycles (FPGA Loop)

• Real-Time VI – a virtual instrument operated at RT controller including n-number of cycles (RT Loop)

• User Interface VI – a virtual instrument operated at host PC including n number of cycles (UI Loop) providing HMI.

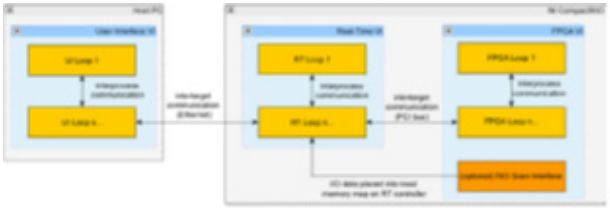

*Figure 6. Architecture of software support with RIO*

In each of the VI, a software connection between elements of the separate cycles is provided. The connection between FPGA and Real-Time is provided through the PCI communication bus, and the connection between Real-Time and Host PC is Ethernet.

A connection for I/O data (RIO Scan Interface) between FPGA and Real-Time is provided, i.e. the use of Real-Time without processing of the FPGA signals.

For realisation of this project was developed two applications: FPGA and Real-Time.

Due to the requirement for scanning frequency ≥90kS/s, the LabVIEW FPGA Interface Mode is used, which is the programming mode that reveals the true power of cRIO through configuration and use of the FPGA in addition to the Real-Time processor. For communication between the FPGA and Real-Time, there is an option to choose between the high-speed direct memory access (DMA) or communication through a single point using controls and indicators.

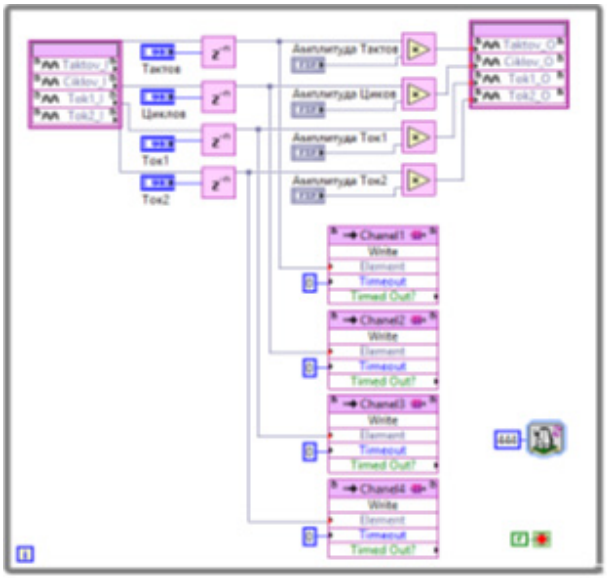

*Figure 7. The application FPGA.*

The application FPGA assuring correction for amplitude and phase, and Real-Time saves settings to non-volatile memory, Figure 7.

## 4. Conclusions

FPGA assure time-delay up to 512 cycles.

The experimental results show that corrections of amplitude and phase are made with easy and without distortion of output signal.

FPGA is ready only 2.5 seconds after restart, and RTOS – after 20 seconds.

## 5. Reference

[1] http://www.ni.com

## Information about the author

Vladimir Lyubomirov Lalev, Engineer, M.Sc., Production automation (1994). Kozloduy NPP plc, Safety and Analysis Section Address: Kozloduy 3320,

Web address: *www.kznpp.org*

*Email address: v_lalev@npp.bg*

**Kiril Iliev Banev,** Engineer, M.Sc., Information and Measurement Equipment (1994). Kozloduy NPP plc, Metrology Assurance, Laboratory for Electrical and Radiotechnical Measurement Address: Kozloduy 3320,

Web address: *www.kznpp.org*

*Email address: kbanev@npp.bg*

**Bisser Ivanov Borissov,** Engineer, M.Sc., Communication and Safety Equipment (2010). Kozloduy NPP plc, Metrology Assurance, Laboratory for Electrical and Radiotechnical Measurement Address: Kozloduy 3320,

Web address: *www.kznpp.org*

*Email address: biborisov@npp.bg*